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MODELING AND TESTING OF FAULTS IN 2TG1M MEMRISTOR MEMORIES

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ABSTRACT

Recently, memristor memory has drawn attention as an attractive option for future non-volatile memories due to its high density, low power consumption and long retention time. However, memristor memory has high defect density due to its nanoscale fabrication and it also suffers from sneak path problem owing to its crossbar architecture. In this paper, fault models for 2TG1M (2 Transmission Gates and 1 Memristor) memory are proposed. A new fault Write Disturbance Fault is analyzed. Additionally, a March Test is proposed to cover the defined faults. The proposed March test requires 5mn read and 5mn write operations for mxn (m words x n bits) 2TG1M memory.

KEYWORDS: Memristor, Test, Fault Models